

the insulating material layer defines an opening, the diffusion barrier layer covers the insulating material layer in the opening, the conductor covers the diffusion barrier layer in the opening, the first material layer includes at least a part of one of the understructure and the insulating material layer, and the second material layer includes at least a part of the conductor.

**13.** The multilayer structure of claim **1**, further comprising:

an adhesion layer between the diffusion barrier layer and one of the first and second material layers.

**14.** The multilayer structure of claim **13**, wherein the adhesion layer includes at least one metal selected from the group consisting of molybdenum (Mo), tungsten (W), niobium (Nb), vanadium (V), tantalum (Ta), titanium (Ti), zirconium (Zr), hafnium (Hf), technetium (Tc), rhenium (Re), ruthenium (Ru), cobalt (Co), palladium (Pd), platinum (Pt), copper (Cu), gallium (Ga), indium (In), tin (Sn), germanium (Ge), and lead (Pb).

**15.** The multilayer structure of claim **13**, wherein the metal in the adhesion layer is the same as a metal in the diffusion barrier layer.

**16.** The multilayer structure of claim **1**, wherein the diffusion barrier layer includes different types of a plurality of 2D material layers, and

a first 2D material layer among the plurality of 2D material layers includes the non-graphene based 2D material.

**17.** The multilayer structure of claim **1**, wherein at least a part of the multilayer structure is an interconnection for an electronic device.

**18.** A device comprising:  
the multilayer structure of claim **1**.

**19.** An electronic device comprising:  
an understructure;  
an insulating material layer on the understructure, the insulating material layer defining an opening;  
a diffusion barrier layer that covers the opening of the insulating material layer, the diffusion barrier layer including a non-graphene-based two-dimensional (2D) material; and  
a conductor on the diffusion barrier layer in the opening.

**20.** The electronic device of claim **19**, wherein the 2D material includes a metal chalcogenide-based material having a 2D crystal structure.

**21.** The electronic device of claim **20**, wherein

the metal chalcogenide-based material includes at least one metal element selected from the group consisting of molybdenum (Mo), tungsten (W), niobium (Nb), vanadium (V), tantalum (Ta), titanium (Ti), zirconium (Zr), hafnium (Hf), technetium (Tc), rhenium (Re), ruthenium (Ru), cobalt (Co), palladium (Pd), platinum (Pt), copper (Cu), gallium (Ga), indium (In), tin (Sn), germanium (Ge), and lead (Pb), and

the metal chalcogenide-based material includes at least one chalcogen element selected from the group consisting of sulfur (S), selenium (Se), tellurium (Te), and oxygen (O).

**22.** The electronic device of claim **19**, wherein the diffusion barrier layer has a thickness of greater than 0 nm and less than or equal to about 5 nm.

**23.** The electronic device of claim **19**, wherein

the understructure includes a semiconductor region, and the diffusion barrier layer limits a material from diffusing between the semiconductor region and the conductor.

**24.** The electronic device of claim **19**, wherein the diffusion barrier layer limits a material from diffusing between the insulating material layer and the conductor.

**25.** The electronic device of claim **19**, further comprising:  
an adhesion layer between the diffusion barrier layer and the conductor.

**26.** The electronic device of claim **19**, comprising:

an interconnect portion, wherein

the interconnect portion includes an active device portion on a substrate portion,

the interconnect portion is on the active device portion, and

the interconnect portion includes the insulating material layer, the diffusion barrier layer, and the conductor.

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